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Contract#: LTR. DATED 2/23/90 Mod #: Document : GRANT
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Main project #:

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Project director(s):
UYEMURA J P EE (404)894-2975

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Sponsor/division codes: 203 / 038

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Contract value	8,000.00	8,000.00
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Title: DESIGN FOR SILICON/FERROELECTRIC LIQUID CRYSTAL RETINA

PROJECT ADMINISTRATION DATA

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Security class (U,C,S,TS) : U ONR resident rep. is ACO (Y/N): N
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Equipment title vests with: Sponsor GIT
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Administrative comments -
PROJECT INITIATION, SUBCONTRACT UNDER NSF PRIME - NSF REGULATIONS APPLY;
FIXED PRICE CONTRACT, 3 EQUAL PAYMENTS (NO INVOICING), 1ST PYMT REC'D

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

NOTICE OF PROJECT CLOSEOUT

Closeout Notice Date 07/01/91

Project No. E-21-F57_____ Center No. 10/24-6-R6899-0A0_

Project Director UYEMURA J P_____ School/Lab ELEC ENGR_____

Sponsor DISPLAY TECH INC/BOULDER, CO_____

Contract/Grant No. LTR. DATED 2/23/90_____ Contract Entity GTRC

Prime Contract No. ISI-8961434_____

Title DESIGN FOR SILICON/FERROELECTRIC LIQUID CRYSTAL RETINA_____

Effective Completion Date 901231 (Performance) _____ (Reports)

Closeout Actions Required:	Y/N	Date Submitted
Final Invoice or Copy of Final Invoice	N	_____
Final Report of Inventions and/or Subcontracts	N	_____
Government Property Inventory & Related Certificate	N	_____
Classified Material Certificate	N	_____
Release and Assignment	N	_____
Other _____	N	_____

Comments_____

_____

Subproject Under Main Project No. _____

Continues Project No. _____

Distribution Required:

Project Director	Y
Administrative Network Representative	Y
GTRI Accounting/Grants and Contracts	Y
Procurement/Supply Services	Y
Research Property Managment	Y
Research Security Services	N
Reports Coordinator (OCA)	Y
GTRC	Y
Project File	Y
Other _____	N
_____	N

Design for Silicon/Ferroelectric Liquid Crystal Retina

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June 19, 1991

Final Report
23 February--31 December 1990
Project E-21-F57

Sponsored by
Displaytech, Inc.
2200 Central Avenue
Boulder, CO 80301

Table of contents

Summary

The fabrication of ferroelectric liquid crystal (FLC) light modulators directly atop silicon integrated circuits makes possible a new family of micropower optoelectronic computing elements. These elements benefit from the high circuit complexity now available at low cost in silicon VLSI (very large scale integration), and the fast, low-power light modulation of FLCs.

The work reported here involved the design of two devices that combine FLC light modulator outputs with silicon photodetector inputs and verying degrees of "on-board" processing. The first of these, an optical thresholding array, has a 6×20 array of $130\,\mu$m square elements, each element comprising a photodetector, an adjustable threshold circuit, and an FLC modulator. The array accepts a grey-scale input image, and returns a clipped binary image, with the clipping threshold externally adjustable. We observed 150 A/W photosensitivity, 2 ms response times, and 4% threshold uniformity over the 4×18 elements in the interior of the array. The second device is based on the "silicon retina" of Carver Mead, but adds optical outputs. These "retinas" are CMOS VLSI implementations of neural computers which duplicate many of the functions of the vertebrate retina. The device accepts an input image, and returns a binary image with edges and motion enhanced.

Fabrication of FLC light modulators on all devices was performed by Displaytech, Inc. at their facility in Boulder, CO.

Optoelectronic computing devices such as these should be useful wherever fine-grain, highly interconnected processing is desired. For example, they could perform preprocessing of complex images in real time, with an output available in real time from each pixel for further optical processing. The FLC modulators allow readout at frame rates up to 10 kHz, more or less independent of the number of elements in the device. The superiority of these devices over digital electronics, and especially their low cost, should give them many commercial applications, for example in the fields of machine vision.

Acknowledgements

A large contribution to this work was made by Dr. Mark Handschy of Displaytech, Inc., who participated closely in the conceptual design of the silicon devices, and in their testing and characterization.

The fabrication by Displaytech of FLC light modulators on the VLSI chips was an enabling element in the research, without which no interesting experimental results could have been demonstrated.

1. Introduction

Neural computers are of current interest because they may be able to solve problems that confound stored-instruction digital computers. Much of today's research on neural networks centers on how they can learn, but, even without learning, biological neural systems prove that there exist simple solutions to computational problems that are difficult to solve digitally. For example, processing of visual images is performed elegantly in the vertebrate retina, but is quite cumbersome on digital computers.

Carver Mead has constructed an analog VLSI (very large scale integration) silicon ship that models some of the primitive functions of the retina [1, 2]. This "silicon retina" comprises an array of logarithmic photodetectors connected by a resistor network that computes a spatially and temporally averaged representation of the input image. Amplifying the difference between the photodetector outputs and the averaged image produces edge and motion enhancement. By representing input intensities as analog currents and voltages, many of the computational problems such as aliasing and numerical instabilities associated with sampled representations are avoided. Thus, the silicon retina is very compact, yet solves in a few milliseconds problems that even much larger digital computers have trouble solving in many seconds. However, Mead's retina is read out serially, incurring a substantial overhead. The scanning process requires sampling each picture element at discrete times, which can negate the previously mentioned advantages if subsequent computation is to be performed on the output. As the readout rate increases, the power dissipated in toggling the address lines quickly comes to dominate the total power consumption of the device.

These problems can be solved by providing parallel readout in the form of a light modulator for each retina cell. Since the real-time, analog neural computation model requires modest bandwidth, the mature and VLSI-compatible technology [3] of liquid crystal light modulators suits the interconnection purposes of the retina.

2. Optical thresholding array

A schematic diagram of the thresholding device appears in Fig. 1. It is a square array of identical cells, each of which comprises a phototransistor detector, static CMOS inverter, and FLC modulator cell. The array performs a binarization, or thresholding, operation on an incident image. A bias level of the NMOS load transistor Q_{b} in each detector is established by injecting a current I_0 via a package pin through a single NMOS transistor Q_{B}; the level of gate voltage required to sustain that current is broadcast to the NMOS load device in every cell. The input node of the inverter A is charged by the emitter current I_{ph} of the n-p-n phototransistor Q_{ph}, which current is proportional to input light intensity, and

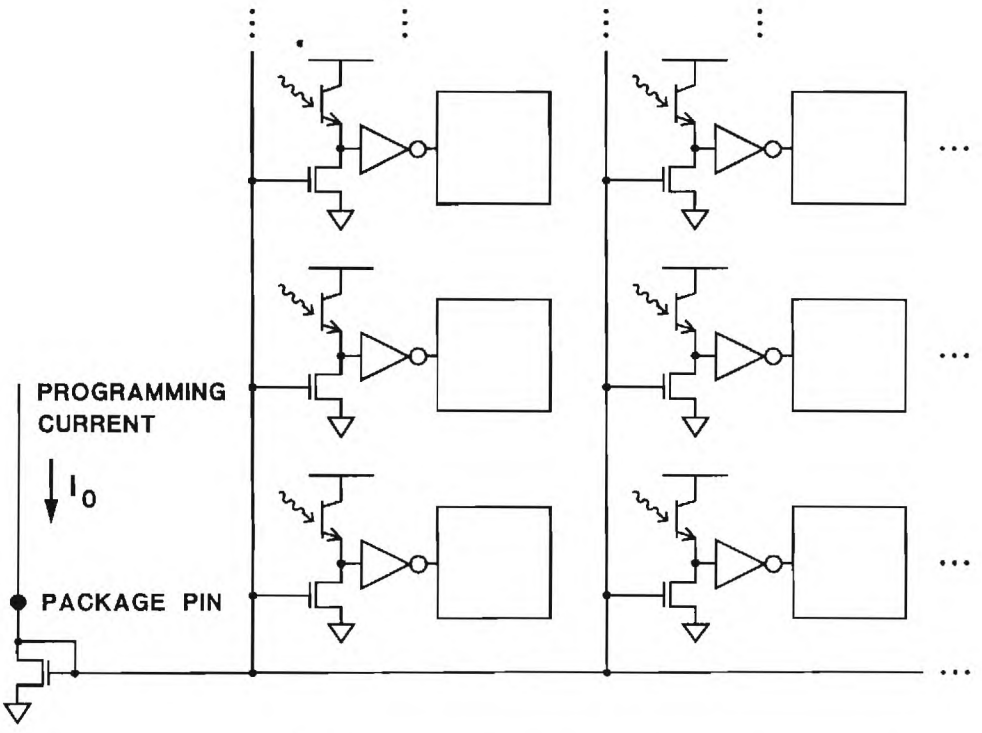

Figure 1: Schematic diagram of fabricated Si/FLC-based optical thresholding device. A single switching threshold for all cells is programmable by means of a reference current supplied through a package pin.

discharged by the bias current I_b through Q_b, which is $\sim I_0/3$ due to the ratioing of transistor gate widths. Thus the inverter's input node accumulates positive charge when I_{ph} exceeds I_b and discharges when I_b exceeds I_{ph}. The high gain of inverter A about its threshold point near 2.5 V drives its output—and thus the FLC modulator pad—quickly to 0 or 5 V for small values of $|I_{ph} - I_b|$.

A 20×6 array of these cells was fabricated on a 130 μm pitch in the 3 μm, p-well CMOS technology available through the MOS Implementation Service (MOSIS) [4]. The array operates from a 5 V supply with the common transparent electrode held at 2.5 V. The array size was determined by space remaining on a die devoted to another design. Cell assembly and filling were performed as described in Ref. 3. Figure 2 shows a reflection photomicrograph of a portion of the cell array taken under gradient illumination. The phototransistor active area is the small dark square in the center of each cell. The modulator electrode is a square pad covering the cell with a 32×35 μm hole in its center to admit the input light. The three MOS transistors in each cell are beneath the modulator electrode. Figure 2 shows the device performance at bias current $I_0 = 17\,\mu$A, with an illumination intensity gradient on the device. Cells in the less illuminated portion of the array are below threshold and turn completely off. Speed measurements were conducted on a representative cell

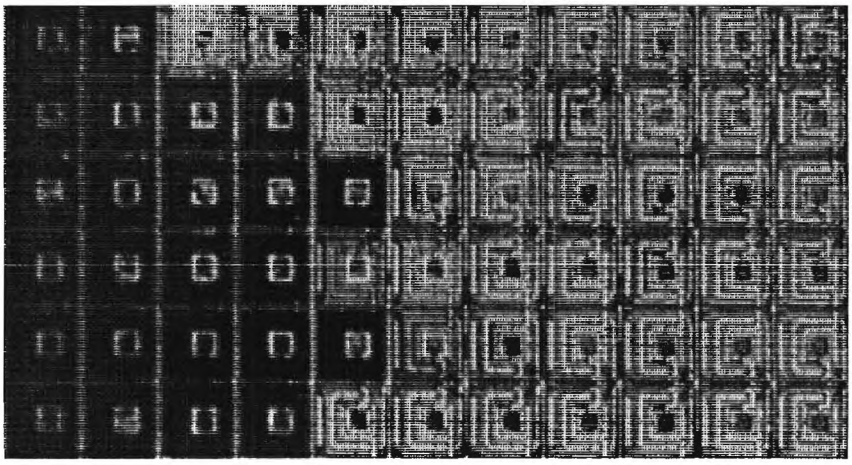

Figure 2: Portion of the thresholding array under gradient illumination: bias current $I_0 = 17\mu$A; dimly illuminated elements completely off.

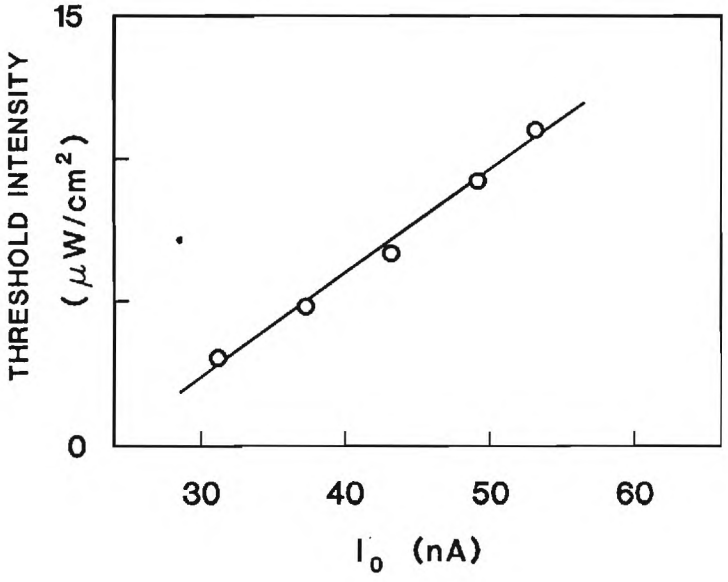

Figure 3: Threshold intensity *vs.* bias current for a typical thresholding cell. Data indicate a roughly linear variation of threshold with programming bias current.

excited by toggling a $100\,\mu\mathrm{W/cm^2}$ green light source on and off with bias current I_0 set at $3.9\,\mu$A. Measurements of delay from the rising or falling edge of the input intensity to 90% of the total response yielded a turn-on time of 1.5 ms and a turn-off time of 2.0 ms, respectively.

The variation of optical switching threshold with bias current is illustrated in Fig. 3. An approximate value for the phototransistor responsivity of 150 A/W

can be inferred from these data and the size of the opening in the metal above the detector. The variation of threshold point with bias current is approximately linear. However, the threshold is not uniform over the entire array. Cells on the periphery of the array appear to be more sensitive than the interior cells [5]. We believe this behavior arises from diffusion of photoexcited charge carriers from exposed regions of bulk silicon surrounding the array into the base regions of the phototransistors, which all share the bulk as a collector. Indeed, measurements conducted on similar photosensitive elements from an earlier MOSIS fabrication run [6] indicate that light incident several tens of microns away from a junction causes photocurrent to flow. This can occur by virtue of the long minority carrier lifetimes and diffusion lengths in good quality bulk silicon [7]. Receptor sensitivity can be localized through electrical isolation of the photosensing devices. Junction isolation of photodiodes is possible in the standard MOSIS n-well or p-well processes [6], and junction isolated vertical transistors are available in the new MOSIS low noise analog process [4, 8].

If only elements in the interior of the array are considered, the standard deviation of the threshold point current about its mean value of $9.73\,\mu$A is $0.35\,\mu$A or $\sim 4\%$. With some design refinement to obtain better matching of cell threshold characteristics, such an array could be used in image processing applications where a precise programmable thresholding operation is desired.

The elements of the array described above combine a single-transistor current source load with a two-transistor inverter to make a current comparator with a sharp threshold. Operations that are much more complex and interesting can be achieved with only modestly more electronic components, as demonstrated by the example of the silicon retina presented below.

3. Silicon/FLC retina

A goal of the research has been to realize an IC/FLC device that more fully exploits the sophisticated functionality available from silicon VLSI circuitry; adding optical readout to Carver Mead's silicon retina was a natural choice.

3.1 Optoelectronic retina: design

The design of the retina was adapted directly from Ref. 2, substituting FLC drivers for Mead's electronic output lines, as shown in the schematic diagrams of Fig. 4 The FLC driver performs two functions. First, the output of the differential transconductance amplifier is a current which the driver converts to voltage for the FLC. Second, the retina's edge enhancement action produces a bipolar response near an edge. Since the FLC light modulator has a binary response, only one sign of the edge enhancement can be distinguished from the background. Therefore, the FLC

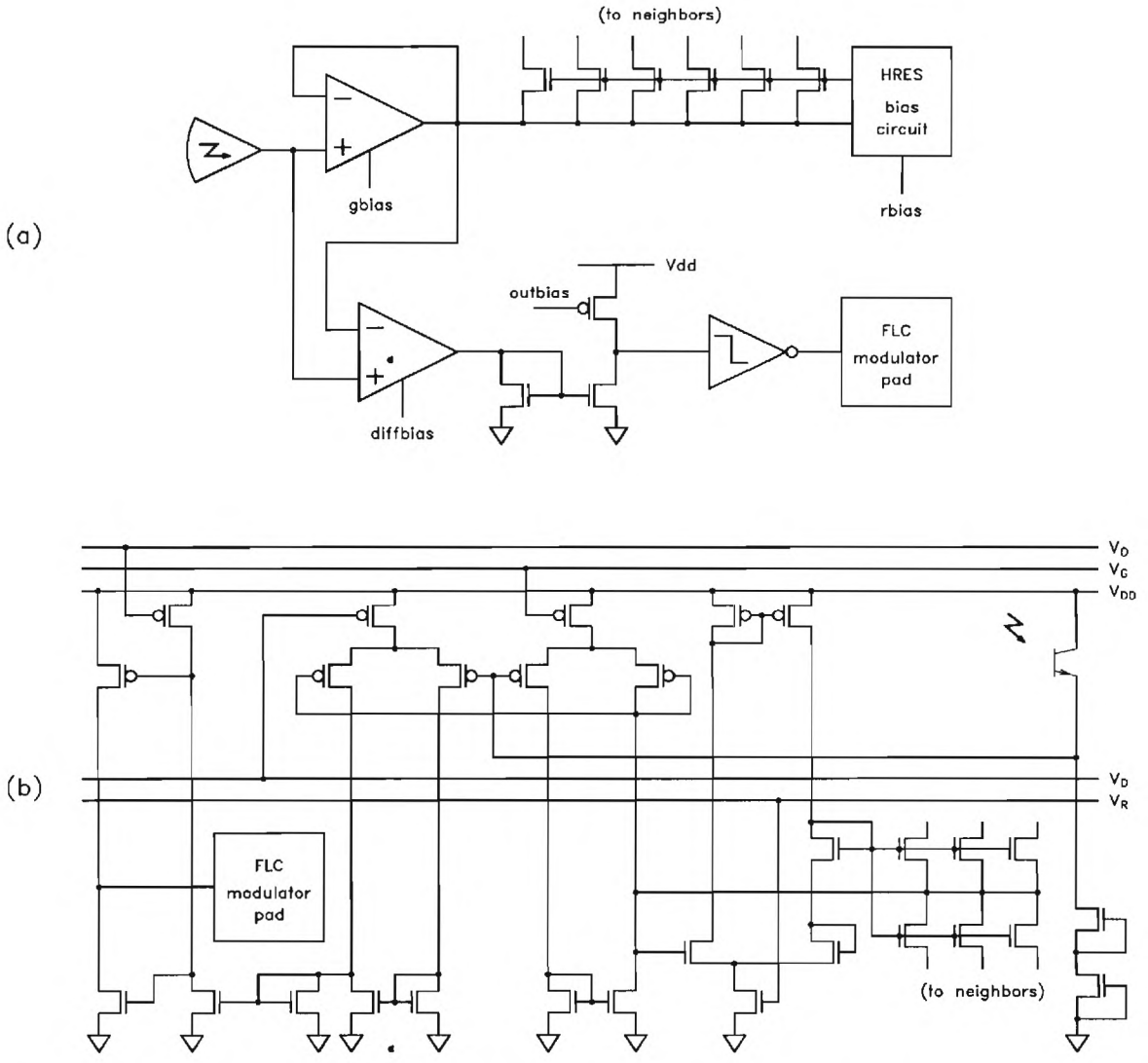

Figure 4: (a) Block diagram of FLC retina element. The circuit is the same as that of Mead *et al.* up to the output of the differential amplifier. Following the amplifier is a rectifier that drives the FLC modulator pad. (b) Transistor level schematic. The voltages V_O, V_G, V_D, and V_R control the rectifier threshold current, the transconductance of the buffer amplifier, the transconductance of the differential amplifier, and the conductance of the resistors in the network, respectively.

driver also half-wave rectifies the retina output. These functions are performed in the following way: the pMOS transistor sources a constant current I_O determined by the external programming voltage V_O. This current is subtracted from the output current I_D of the differential amplifier by the current mirror comprising the two nMOS transistors. The difference of the two currents charges (or discharges) the input capacitance of the conventional CMOS inverter, whose output in turn drives

the large metal pad which functions as both FLC driving electrode and mirror. Since I_O must be nonnegative, the pad can be driven to +5 V only for sufficiently positive I_D; otherwise the pad is driven to 0 V.

A complete transistor-level schematic of a single retina element is shown in Fig. 4(b). The sizing of the transistors for the portion of the circuit up to the FLC driver is greatly indebted to layouts published as the endpapers of Mead's book [2].

Cells were tiled on an hexagonal lattice to form the complete retina layout. Each cell occupies a rectangle of size $97 \times 112\,\lambda$, where λ is a unit of length equal to half the smallest feature size permitted by the integrated circuit design rules. The $2\,\mu$m CMOS process in which the FLC retina was fabricated has $\lambda = 1\,\mu$m. The rectangle dimensions approximate the ratio $1 : \sqrt{3}/2$ to within 1 part in 10^4. As much of the surface of the chip as is practical is left covered with the final aluminum layer (metal2). This layer serves to block light from the purely electronic portions of the circuitry as well as to form the FLC modulator's reflective driving pad. The FLC contacts the pad through an opening in the transparent passivation glass which is the final layer deposited in the IC fabrication process. An opening in the metal2 layer admits light to the phototransistor. A 13×18 array was laid out on a MOSIS TinyChip.

3.2 Optoelectronic retina: fabrication

Whereas previous VLSI/FLC devices had been successfully fabricated [3], the procedure had been performed on medium-sized dice, with approximately 5×7 mm of payload area. The retina design was fabricated through MOSIS on a TinyChip, the smallest available die, with 2.22×2.25 mm of payload area. The use of this convenient and very inexpensive evaluation vehicle was enabled by the development by Displaytech, Inc. of a proprietary method for the fabrication of FLC modulators on these extremely small dice.

3.3 Results

Two of the four TinyChips arriving from MOSIS were fabricated into FLC devices by Displaytech. Figure 5 shows a photograph of the cavity of an assembled FLC device.

3.3.1 Experimental setup

The devices were evaluated at Displaytech using a polarized light reflection microscope. The microscope was configured to augment the usual uniform illumination over the entire device with a moveable uniformly bright region that facilitated the excitation of the device with an edge of variable contrast.

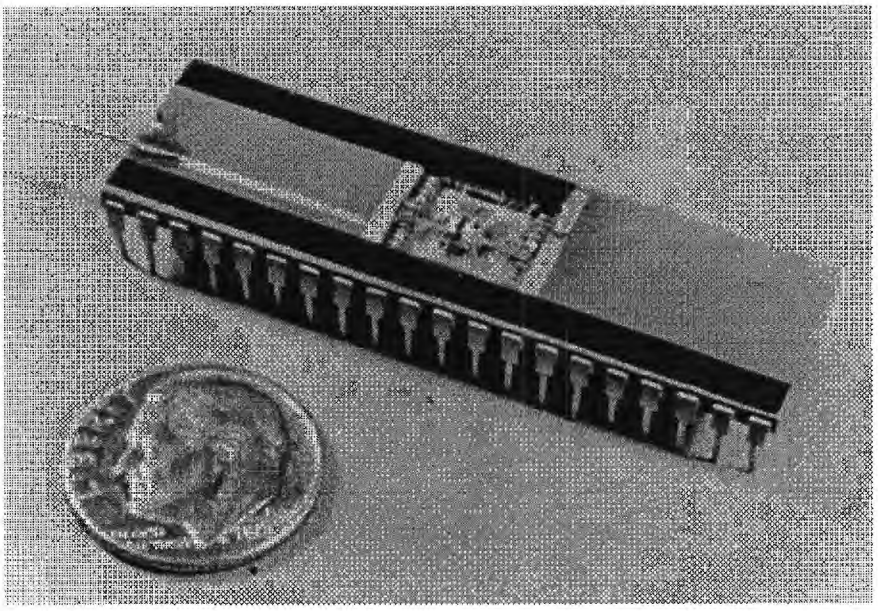

Figure 5: Photograph of assembled FLC/TinyChip retina device. The dime shows the scale.

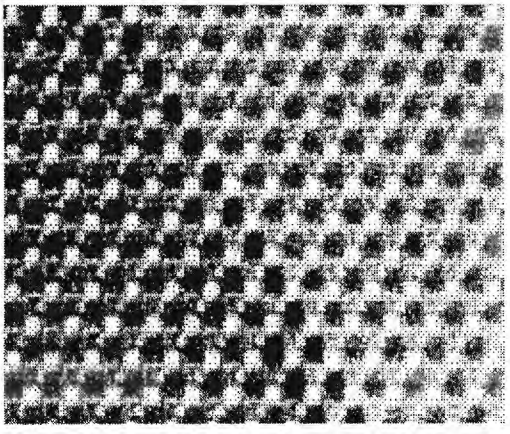

Figure 6: Photomicrograph of FLC retina showing the edge response. The upper right portion of the retina is illuminated slightly more strongly than the remainder. The switched elements are darker than the unswitched ones.

3.3.2 Retina performance

Establishing retina operating parameters proved a formidable task, as the parameter space has six dimensions: horizontal resistor bias V_R, buffer amplifier transconductance bias V_G, differential amplifier transconductance bias V_D, FLC driver rectifier threshold bias V_O, and the two illumination levels. The procedure

that led to a workable setting of the parameters began with the establishment of very high lateral conductance, which forced the network-stored image to a single DC level. Approximately half the pixels were illuminated at a base level, and the remaining half slightly more strongly. The differential amplifier bias and rectifier threshold bias were then adjusted to produce a binarized output, much like that of the thresholding array discussed previously. Finally, V_G and V_R were tuned until only the modulators in a strip on one side of the illumination edge were switched. Figure 6 shows a photograph of the retina's response to a weak illumination edge. The more strongly illuminated half of the retina received about $150\,\mu\mathrm{W/cm^2}$, while the weakly illuminated half received about $100\,\mu\mathrm{W/cm^2}$. The bias levels were as follows: $V_R = 0.55\,\mathrm{V}$, $V_O = 0\,\mathrm{V}$, $V_D = 0.54\,\mathrm{V}$, and $V_G = 0.40\,\mathrm{V}$.

Operation of the retina with illumination by a moving contrast edge confirmed its ability to detect motion. Biases could be adjusted so that still illumination with an edge produced no switched pixels, but motion of the edge resulted in switching of the pixels at the edge.

4. Conclusion

Working silicon devices have been designed for integration with ferroelectric liquid crystals to realize optoelectronic components with optical inputs and outputs. A great advantage of silicon/FLC technology is that the constituent technologies are sufficiently mature that devices can be implemented without further development. The prototype designs exhibit the full range of functionality available in silicon VLSI, which supports the thesis that cells of arbitrary design can be implemented as easily as the prototypes chosen for this work.

Silicon CMOS technology and FLC materials are favorably matched with respect to fabrication compatibility and drive requirements. Switching energies of FLC materials are typically a few $\mathrm{fJ}/\mu\mathrm{m}^2$, and switching speeds in the tens of microseconds can be contemplated for FLC modulators driven from a silicon VLSI die. Although CMOS logic speeds are much higher than FLC switching rates, the low static power dissipation of silicon CMOS logic permits a subpicojoule speed-power product to prevail at low clock rates. This reciprocity allows CMOS circuitry to be operated at rates matching liquid crystal switching times (10^3 –10^5 Hz) without suffering an increase in switching energy. Because the switching energy of an FLC modulator is comparable with that of a few transistors, total power dissipation of silicon/FLC devices can be of the same order as a silicon CMOS chip operating at 10–100 kHz clock rates. Moreover, the great degree of concurrency (fraction of elements switching at the same time) attainable in fine-grain parallel-readout systems can still yield high throughput at these clock rates.

We therefore foresee applications of silicon/FLC optoelectronic technology in areas where massive parallelism and low power operation at moderate speeds may

be suitable, such as special purpose image processing systems, realizations of early vision models, [2, 9] and optoelectronic neural networks. Additionally, the ability to use standard VLSI fabrication processes as a basis for these devices renders them suitable for low cost fast-turnaround construction of prototypes for systems in which the ultimate light modulator technology may be different.

4.1 Further work

The work reported here embodies merely a demonstration of the silicon/FLC concept. Extensive characterization of the electrical performance of the VLSI circuitry is necessary before serious progress can be made toward practical devices. Test structures present on the existing chips should be evaluated thoroughly to confirm operation according to the retina cell model and to resolve questions raised by certain observed behaviors.

With better electrical characterization of the retina cell, a desirable next step is to fabricate a larger array; 80×80 is possible on the largest standard MOSIS die if the $\lambda = 1\,\mu$m feature size is retained. 200×200 arrays are possible in $0.6\,\mu$m technology; however a new sequence of small test chips would need to be fabricated for circuit verification.

4.2 Commercial applications

Likely first applications for the technology demonstrated in this work are in the field of image processing. Solutions to many seemingly simple problems relevant to machine vision and robotics are computationally demanding when implemented on digital machines. Examples are the types of 2-D nonlinear filtering operations inherent in current approaches to pattern recognition, for example, realizing models of the early biological vision system [9] and mathematical morphology [10].

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